UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/543,173	07/22/2005	Masaki Yamada	274300US2PCT	7941

22850 7590 09/29/2008

OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
CAVALLARI, DANIEL J	

ART UNIT	PAPER NUMBER
2836	

NOTIFICATION DATE	DELIVERY MODE
09/29/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentdocket@oblon.com
oblonpat@oblon.com
jgardner@oblon.com

Office Action Summary	Application No.	Applicant(s)	
	10/543,173	YAMADA ET AL.	
	Examiner	Art Unit	
	DANIEL CAVALLARI	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 July 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/22/2005,5/30/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement(s) filed 5/30/2007 and 7/22/2005 have been considered.

Claim Objections

Claims 4, 10, and 16 are objected to because of the following informalities:

In regard to claim 4

The sentence "so that their output voltage which are different each other are superimposed" is grammatically incorrect.

Appropriate correction is required.

In regard to claims 10 and 16

There is a lack of antecedent basis for the terms "the current" and "the normal conditions".

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 4, 5, 7, 8, 10, 11, and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In regard to claim 1

1. The claim states "a straightforward switch **connected in series with a system** which connects a power source to a load" and further states "a first single phase inverter **connected in parallel with said system**" and "a second single phase inverter **connected in series with said system**" and continues to reference "said system". However, applicant fails to identify in the claim, specification, or drawings what "said system" is in reference to. The claim states that "the system" is **"a system which connects a power source to a load"**. This description appears to equate to the entire device attached to load (2) of figure 1, however such an interpretation renders the claims meaningless. If "said system" was the entire device, then the claims describe how the "system" is connected to itself. An element described as "parallel" or "in series" is meaningless unless first given a frame of reference to which the description can be attached. Therefore, the "series" and "parallel" labels given in the claims is meaningless and will be read on by any electrical connection.
2. The claim recites "a first single phase inverter" and "a second single phase inverter". An inverter is a well known device in the electrical art that converts a DC voltage to an AC voltage. The specification discloses that "The single phase inverters 4, 5 are operated as a rectifier and charge the battery." A rectifier, as known in the art, converts DC power to AC power. Therefore, the "inverter" is not actually an "inverter" as commonly referred to in the art by a bi-directional converter that performs both inverting and rectification.

In regard to claim 4

The claim state "output voltages which are different each other [sic] are superimposed **and** supplied to the load." However, figure 1 depicts a device wherein the superposition occurs **at** the load.

In regard to claim 5

The sentence "after decreasing in the system voltage" is grammatically incorrect.

The term "pseudo-sinusoidal voltage wave" is not one ordinarily used in the art to refer to a particular voltage waveform. The distinction between a "pseudo-sinusoidal voltage wave" and a real or actual pseudo-sinusoidal voltage wave is unclear. Therefore, the claim will be read on by any voltage waveform.

In regard to claim 7

The phrase "and receive energy through the DC-DC converter between both inverters" is confusing.

In regard to claim 8

The phrase "connected in series each other" is grammatically incorrect.

In regard to claims 10 and 16

It is unclear what is meant by "reactive power in the normal condition is **flown** in or out from the system". The claim will be interpreted as best understood to be red on by any converter that provides reactive power compensation.

Since "the system" was not adequate disclosed in claim 1, it is unclear where the current is being "flown" from.

In regard to claim 11

The claim states the "single phase inverter is PWM-controlled so that the direct current (DC) voltage of the second single phase inverter [noting that an inverter converts DC to AC power] is 0.5 or more [noting that 0.5 lacks any reference of units or comparison] of the direct current (DC) voltage of the single phase inverter generating the least voltage out [again, noting that in inverter converters DC to AC power so it is unclear what is meant by some form of comparison of a **"direct current"** voltage from an AC output device.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the particular interconnections of the converters (4, 5, figure 1) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Since the particular interconnection of the device is explicitly claimed, the drawings must provide an accurate representation of the invention incorporating the specific interconnections of the converters (4-7).

Figure 8 fails to adequately show "the first single phase inverter comprised of a plurality of inverters connected in series each [*sic*] other", as claimed in claim 8. The figure shows a plurality of blocks (inverters) interconnected in what appears to be a quasi parallel/series connection but since the details of the inverters themselves are lacking, it is impossible to tell exactly how they are connected. It is further noted that a "parallel connection" is defined in the art as a method of connecting components or circuits so that they share the same voltage, the current dividing between the circuits depending on their impedance" and a "series connection" is defined as "a method of connecting components or circuits so that they share the same current, the voltage dividing between them depending on their impedance" (see "Newnes Dictionary of Electronics"). Since the inverters (4) of figure 8 comprise their own storage devices (capacitors, C) is appears they do not share the same current but rather comprise their own current sources in addition to any shared current.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an

application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 5, 13, and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Keizo et al. (JP11-178216).

In regard to claim 1

A power supply apparatus comprising:

a straightforward switch (3, figure 1) which connects a power source (1) to a load (3), and supplying or interrupting an electric power served from the power source to the load [read on by opening and closing the switch];

a first single phase inverter (6);

a second single phase inverter (4); and

a direct current output means (5) connected to direct current side terminals of said the first and second single phase inverters (see figure 1)

In regard to claim 2

The power supply apparatus according to claim 1, wherein said second single phase inverter (4) is connected between the first single phase inverter and the load (see figure 1).

In regard to claims 5 and 14

Wherein the first and second single phase inverters form a pseudo- sinusoidal voltage wave comprising a voltage waveform having a plurality of output levels [noting that an alternating current alternates between a plurality of voltage levels) to output it to the load, by combining their output voltages (0 volts from inverter 6 and full voltage from inverter 4, figure 1) after decreasing in the system voltage and opening of the straightforward switch (see paragraph 7).

Claim 13

The power supply apparatus according to claim l, wherein said second single phase inverter is connected between said first single phase inverter and the power source (see figure 1).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 7, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keizo et al. (hereinafter referred to as Keizo) in view of Oughton, Jr. (US 6,753,622).

In regard to claims 3 and 7

Incorporating all arguments above, Keizo fails to teach either of the inverters connected to a DC-DC converter.

Oughton teaches a power supply system wherein an either the DC source (20) is connected to the inverter (822) via a DC-DC converter (824).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate a DC-DC converter between the battery and inverter as taught by Oughton into the system of Keizo. The motivation would have been to better regulate the battery voltage and given the system flexibility with the ability to power the system with a battery voltage different than the DC operating voltage

In regard to claim 12

Keizo further teaches:

wherein the direct current voltage of said second single phase inverter is changed by said DC-DC converter according to an amount of decreased or increased system voltage (see paragraph 5).

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Keizo et al. (hereinafter referred to as Keizo) in view of Ozawa (US 5,866,506).

Incorporating all arguments above, Keizo fails to explicitly teach superimposing different voltages at the load to provide the drive for the load. Ozawa teach superimposing different voltages at the load creating a drive voltage (See figure 5B).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide different voltages at the load from the inverters of Keizo as taught by Ozawa. The motivation would have been to provide the load with a drive voltage (noting that if the voltage provided is the same voltage (potential) then there is no drive voltage and no power or drive to operate the load).

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Keizo et al. (hereinafter referred to as Keizo) in view of Sakai (US 6,034,514).

Keizo teaches the second inverter equalizing harmonic current but fails to explicitly teach the converter superimposing voltage for compensation by pulse width modulation or voltage value. Sakai teaches a power supply apparatus wherein pulse width modulation is used to adjust for voltage fluctuations (see Column 3, line 55 to column 4, line 11). It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the PWM technique for adjusting for fluctuations as taught by Sakai into the system of Keizo. The motivation would have been to use a well known and established method of voltage control to compensate for fluctuations in the voltage.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Keizo et al. (hereinafter referred to as Keizo) in view of Bong-Hwan et al. ("Improved Single-Phase Line-Interactive UPS).

Incorporating all arguments above, Keizo teaches a switch (2, figure 1) but fails to explicitly teach what the switch is made of. Bong-Hwan et al. (hereinafter referred to as Bong-Hwan) teach a power supply apparatus comprising a semiconductor switch (see "bypass switch", figure 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the semiconductor switch taught by Bong-Hwan in place of the switch taught by Keizo. The motivation would have been to use a switch well known and readily available.

Claims 8-11 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keizo et al. in view of Vinciarelli et al. (US 5,786,992) (hereinafter referred to as Vinciarelli).

In regard to claim 8

Incorporating all arguments above, Keizo fails to explicitly teach inverters connected in series. However, Vinciarelli teaches connecting converters in series in order to reduce the minimum operating voltage (see column 3, lines 10-18).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the series connected converter configuration as taught by Vinciarelli in

the design of the inverters taught by Keizo. The motivation would have been to reduce the minimum operating voltage.

In regard to claim 9

Vinciarelli further teaches a plurality of converters connected in series with attached DC sources (capacitors, see figure 15) however Keizo and Vinciarelli fail to explicitly teach the DC sources comprising a voltage relationship of 1:2, or 1:3.

However, it would have been an obvious matter of design choice to size the sources in a 1:2 or 1:3 voltage relationship, since such a modification would have involved a mere change in size of a component and change in size is generally recognized as being within the level of ordinary skill in the art. *In re Rose*, 105 USPQ 237 (CCPA 1955).

In regard to claims 10 and 16

Keizo further teaches compensating for reactive power (See abstract).

In regard to claim 11

Vinciarelli further teaches a plurality of converters connected in series with attached DC sources (capacitors, see figure 15) however Keizo and Vinciarelli fail to explicitly teach said second inverter having a DC voltage 0.5 or more of the DC voltage of the single phase inverter generating the least voltage out of a plurality of the inverters constituting the first single phase inverter.

However, it would have been an obvious matter of design choice to size the sources in a 1:2 or 1:3 voltage relationship, since such a modification would have involved a mere change in size of a component and change in size is generally recognized as being within the level of ordinary skill in the art. *In re Rose*, 105 USPQ 237 (CCPA 1955).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel Cavallari whose telephone number is 571-272-8541. The examiner can normally be reached on Monday-Friday 9:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (571)272-2800 x36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Michael J Sherry/
Supervisory Patent Examiner, Art Unit 2836

/Daniel Cavallari/

September 22, 2008